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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,644	HAMA, HIROSHI	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 March 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 4 is objected to because of the following informalities: On page 14, line 5, "first signal" is incorrect. It should be --second signal--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 3, 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Makihara et al. (US 5,383,205).

Makihara et al. anticipate claim 1.

Makihara et al. teach an error detection and correction circuit for detecting and correcting an error in an input signal containing a first signal and a second signal (figure 2, col. 12, lines 21-25, Makihara et al.), comprising:

A selection circuit for selecting either the first signal or the second signal in the input signal (data selector 113 in figure 2, col. 12, lines 18-20, Makihara et al.);

An error detection and correction circuit unit for detecting and correcting an error in an output signal from the selection circuit (figure 2, col. 12, lines 21-25, col. 19, lines 45-48, Makihara et al.), and

A switch circuit for outputting an output signal from the error detection and correction unit to either an output path for the first signal or an output path for the second signal (figure 2, col. 13, lines 38-39, lines 67-68).

- Makihara et al. anticipate claim 2.

Makihara et al. teach that the error detection and correction unit has a memory storing the first signal and the second signal (col. 11, lines 53-56, col. 12, lines 1-3, Makihara et al.).

- Makihara et al. anticipate claim 3.

Makihara et al. teach that the memory has a first predetermined area storing the first signal and a second predetermined area storing the second signal (col. 12, lines 1-3, lines 12-14, Makihara et al.).

- Makihara et al. anticipate claim 4.

Makihara et al. teach that the error detection and correction unit receives the first signal when the first signal is supplied, and conducts error correction to the first signal received, and the error detection and correction unit receives the second signal when the second signal is supplied, and conducts error correction to the second signal received (figure 2, col. 12, lines 18-21, lines 27-28, Makihara et al.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara et al. (US 5,383,205) as applied to claim 1 above, and further in view of Nibby, Jr. et al. (US 4,077,565).

As per claim 5, Makihara et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Makihara et al. do not explicitly teach that the first signal occupies a larger portion of the input signal than the second signal.

Nibby, Jr. et al. in an analogous art teach that data bit signals RD8 and RD9 are unequal (col. 6, lines 51-54, Nibby, Jr. et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Nibby, Jr. et al. by including additionally that the first signal occupies a larger portion of the input signal than the second signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the first signal occupying a larger portion of the input signal than the second signal would provide the opportunity to use a faster processor to process the first signal and a slower processor to process the second signal.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara et al. (US 5,383,205) as applied to claim 1 above, and further in view of Hatta (US 6,618,450 B1).

As per claim 6, Makihara et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Makihara et al. do not explicitly teach that the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.

Hatta in an analogous art teaches that FIG. 5 shows an example of a receiving apparatus for digital satellite broadcasting corresponding to the transmitting apparatus shown in FIG. 1. The transmitting code decoding apparatus 140 comprises an energy dispersal signal removing circuit 133 for decoding the TMCC signal and a deinterleaver 136 for decoding a data stream (figure 1, 5, col. 6, lines 33-35, lines 39-44, Hatta).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Hatta by including additionally that the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to process both the main signal and the TMCC signal using a single error correction circuit.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara et al. (US 5,383,205) as applied to claim 1 above, and further in view of Hagiwara et al. (US 5,095,417) and Yamaguchi et al. (US 5,737,022).

As per claim 7, Makihara et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Makihara et al. do not explicitly teach that the error detection and correction signal sets a completion flag upon completion of error detection and correction with respect to the first signal received.

Hagiwara et al. in an analogous art teach that an error check completion signal from the error checking circuit 405 and ERR' sending completion signal from the ERR' generating circuit 409 (figure 11, col. 12, lines 53-56, Hagiwara et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Hagiwara et al. by including additionally that the error detection and correction signal sets a completion flag upon completion of error detection and correction with respect to the first signal received.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to send another signal to the error correction circuit for processing.

Makihara et al. also do not explicitly teach that the selection circuit supplies the second signal to the error detection and correction unit when the selection circuit receives the second signal and detects the completion flag.

However Yamaguchi et al. in an analogous art teach that the mode determination circuit 147 may be constructed to supply a signal to cause the selector 147 to output an input from the pixel value interpolation circuit 145 without fail when a scene change identifying flag is transmitted from the transmission side (figure 22, col. 19, lines 50-55, Yamaguchi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Yamaguchi et al. by including additionally

that the selection circuit supplies the second signal to the error detection and correction unit when the selection circuit receives the second signal and detects the completion flag.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to process two different signals using the same error detection and correction circuit.

- As per claim 8, Makihara et al., Hagiwara et al. and Yamaguchi et al. teach the additional limitations.

Makihara et al. teach that the error detection and correction unit calculates a syndrome based on the input signal, processes the syndrome calculated to calculate an error position polynomial and erroneous value polynomial, and conducts error correction based on the error position polynomial calculated and the erroneous value polynomial calculated (syndrome signal generator 110, correction signal generator 111 in figure 2, col. 12, lines 21-27, lines 31-40, Makihara et al.).

Hagiwara et al. teach that the error detection and correction unit sets the completion flag upon completion of calculation of an error position polynomial and an erroneous value polynomial with respect to the first signal (figure 11, col. 12, lines 53-56, Hagiwara et al.).

9. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara et al. (US 5,383,205), Hagiwara et al. (US 5,095,417) and Yamaguchi et al. (US 5,737,022) as applied to claim 7 above, and further in view of Nibby, Jr. et al. (US 4,077,565).

As per claim 9, Makihara et al., Hagiwara et al. and Yamaguchi et al. substantially teach the claimed invention described in claim 7 (as rejected above).

However Makihara et al., Hagiwara et al. and Yamaguchi et al. do not explicitly teach that the first signal occupies a larger portion of the input signal than does the second signal.

Nibby, Jr. et al. in an analogous art teach that data bit signals RD8 and RD9 are unequal (col. 6, lines 51-54, Nibby, Jr. et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Nibby, Jr. et al. by including additionally that the first signal occupies a larger portion of the input signal than the second signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the first signal occupying a larger portion of the input signal than the second signal would provide the opportunity to use a faster processor to process the first signal and a slower processor to process the second signal.

- As per claim 10, Makihara et al., Hagiwara et al., Yamaguchi et al., and Nibby, Jr. et al. teach the additional limitations. Makihara et al. teach that the selection circuit supplies the second signal to the error detection and correction unit when the selection circuit receives a predetermined number of second signals (col. 12, lines 18-21, Makihara et al.). Hagiwara et al teach detecting the completion flag set (figure 11, col. 12, lines 53-56, Hagiwara et al.).

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makihara et al. (US 5,383,205), Hagiwara et al. (US 5,095,417), Yamaguchi et al. (US 5,737,022) and Nibby, Jr. et al. (US 4,077,565) as applied to claim 9 above, and further in view of Hatta (US 6,618,450 B1).

As per claim 11, Makihara et al., Hagiwara et al., Yamaguchi et al. and Nibby, Jr. et al. substantially teach the claimed invention described in claim 9 (as rejected above).

However Makihara et al., Hagiwara et al., Yamaguchi et al. and Nibby, Jr. et al. do not explicitly teach that first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.

Hatta in an analogous art teaches that FIG. 5 shows an example of a receiving apparatus for digital satellite broadcasting corresponding to the transmitting apparatus shown in FIG. 1. The transmitting code decoding apparatus 140 comprises an energy dispersal signal removing circuit 133 for decoding the TMCC signal and a deinterleaver 136 for decoding a data stream (figure 1, 5, col. 6, lines 33-35, lines 39-44, Hatta).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Makihara et al.'s patent with the teachings of Hatta by including additionally that the first signal is a main signal and the second signal is a TMCC signal, and wherein both are present in a received signal for satellite digital television broadcasting.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to process both the main signal and the TMCC signal using a single error correction circuit.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703)746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Dipakkumar Gandhi
Patent Examiner

Guy J. Lamarre
for

Albert DeCady
Primary Exam[illegible]